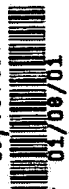


10903 U.S. PTO
09/757404



Class	Subclass	ISSUE CLASSIFICATION

PATENT NUMBER

U.S. UTILITY Patent Application

JCT
67

O.I.P.E. SCANNED <i>HKM</i> Q.A. <i>LAB</i>	PATENT DATE
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APPLICATION NO. 09/757404	CONT/PRIOR	CLASS 703	SUBCLASS 14	ART UNIT 2123	EXAMINER <i>Broda HOGAN</i>
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APPLICANTS

Steven Guccione
Scott McMillan
Brandon Blodget

TITLE

Method and system for device-level simulation of a circuit design for a programmable logic device

PTO-2040
12/99

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)					
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
INTERNATIONAL CLASSIFICATION							

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<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed. <input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent No. _____ <input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	_____ (Assistant Examiner) _____ (Date)			NOTICE OF ALLOWANCE MAILED _____	
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